Design and Simulation of UART for Communication between FPGA and TDC using VHDL

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Abstract—UART(Universal Asynchronous Reciever Transmitter) is a type of serial communication protocol; mostly used for low speed, short distance and low cost data exchange between computer and peripherals. UART includes three important modules which are the baud rate generator, receiver and transmitter. The UART design in this paper is used for communication between FPGA (Field Programmable Gate Array) and TDC (Treatment Delivery Controller). The UART design consists of one start bit, 8 data bit and one stop bit. The VHDL code is written and simulated in XILINX 13.9 and tested using SPARTAN 6LX9 TQG144.

Index Terms—Baud Rate, Configurable Logic Blocks (CLBs), Field Programmable Gate Array (FPGA), Input Output Blocks (IOBs),Serial communication,Treatment Delivery Contoller (TDC), Universal Asynchronous Reciever Transmitter (UART)

1 INTRODUCTION

SERIAL communication is a popular means of transmitting data between a computer and peripheral devices such as a programmable instruments or even another computer. Serial communication uses a transmitter to sends data, one bit at a time, over a single communication line to a receiver. This is contrast to parallel communication, where all the bits of each symbol are sends together. Serial communication buses are becoming more common as improved technology enables them to transfer data rate at high speeds.

Serial communication is popular because most computers have one or more serial ports, so no extra hardware is needed then a cable to connect the instruments to the computer or two computers together. Serial communication requires four important parameter: the baud rate, start bit, optional parity bit and stop bit. Asynchronous serial communication has advantages of less transmission line, high reliability and long transmission, therefore is widely used in data exchange between computer and peripherals. Asynchronous serial communication is usually implemented by Universal Asynchronous Reciever and Transmitter (UART) [1]-[2].

A UART is a Universal Asynchronous Receiver Transmitter, which is used to communicate between two devices. Most computers and microcontroller includes one or more serial I/O devices, such as keyboard or serial printer. UART allows full-duplex communication in serial link, thus has been widely used in the data communication and control system. In actual applicatio, usually only a few key features of UART are needed [3].

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2 COMMUNICATION BETWEEN FPGA AND TDC

The UART design has a application in the field of Medical Electronics. The UART design here is for communication between FPGA and TDC.

2.1 FPGA

A FPGA is a digital integrated ciruit that is used to program to do any type of digital function. FPGA has many advantages over the other controller. The advantages are processing of information faster, controller architecture can be optimized for space and speed and it also involve parallel processing.FPGA consist of three major configurable elements: Configurable Logic Blocks (CLBs), Input Output Blocks (IOBs)and Programmable Interconnects. Many manufacturers deliver FPGAs such as Quick logic, Altera, Atmel, Xilinx, etc. In this paper to write and simulate the VHDL code Xilinx 13.9 used. FPGA used in the design is SPARTAN 6 LX9 TQG144 [4].

2.2 TDC

In Medical LINAC for cancer therphyTreatment Delivery Controller (TDC) is used to input all operator commands and consists of a high resolution colour monitor and a dedicated keyboard. The monitor dispalys the treatment parameters that have been entered via dedicated keyboard. Some of the important parameters shown are the selected photon energy, dose, dose rate, time, field size and patient information. The dedicated keyboard is also used to start and terminate the beam and control the mechanical motion. In addition the keyboard incorporates emergency button which when pressed, will shut down all power system. There are many module in the the medical LINAC such as Pulse modulator cabinet, Drive stand, Gantry, Mirror assembly, Collimator etc and to control each module FPGA is used [5]. This FPGA's are interface with the hardware to communicate with the TDC.

3 DESIGN OF UART

UART frame is decided initially and then the communication is started. UART frame format consist of idle bit, start bit, data bits, parity bits and stop bits. Fig. 1 shows the UART frame format for communication.

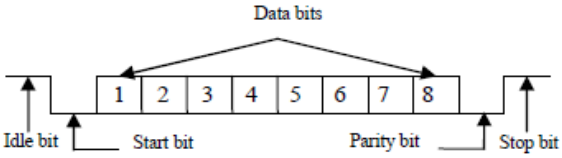

Fig.1 UART frame format

The UARTserial communication module is divided into three sub-modules: Baud Clock, Transmitter module and Reciever module shown in Fig2

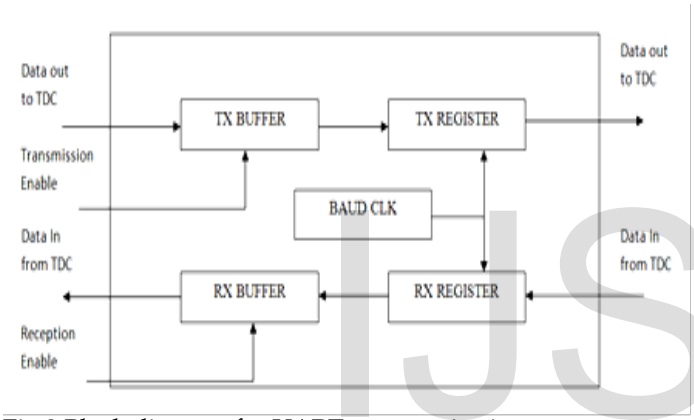

Fig.2 Block diagram for UART communication

4 RESULTS AND DISCUSSION

UART consist of TX buffer and RX buffer. The TX buffer helps in transmission of data with the help of transmission enable signal. The transmission enable signal is enabled only when the enable bit toggle. The RX buffer helps in reception of data with the help of reception enable signal [6].

4.1 Transmission section

The Baud rate set for UART transmission and reception is 115200.

$$Time\ period = \frac{1}{Baud\ clock} \dots\dots\dots (1)$$

Equation 1 shows the time period required according to the baud clock. Hence Time period for 1 bit= 8.62µs, since 8 data bit is required for transmission, one start bit and one stop bit. Therefore total time period for 10 bit to transfer is 8.62*10= 86.2µs. The simulation is based on the first data is enter and then transmission is enable. After enabling the data transmission TI flag is set. For another data transmission makes enable transmission 0 and new data is entered. Again enable transmission is set to 1 to send another data hence it can send data again then make sent flag as 1.
Fig. 3 shows the RTL schematic of the transmission section. It gives a clear view of the data_in and baud clock is labeled as clk then enable_trans shows the enable transmission.

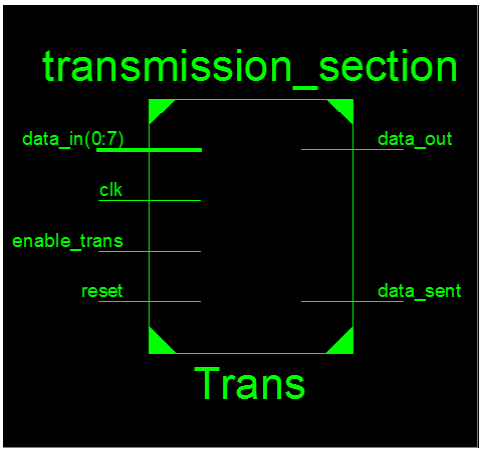

Fig. 3 RTL schematic of the UART transmission section

4.2 Reception section

First input is set to 0 so as to start reception then it is latch till the last bit is received. The important part of UART reception is sampling time is set for baud clock and then data is received. Sampling time is made for better reception to get the required data. When the last bit is received as 1 the data is shifted in. Fig.4 shows the RTL schematic of the UART reception. The RTL schematic shows the clear idea about the UART reception such as the clk and data_in is the input where asdata_out is given to TDC.

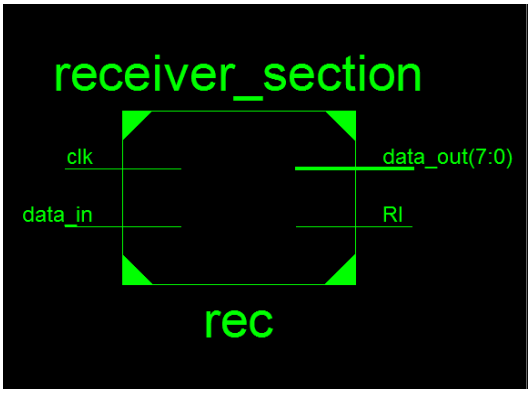

Fig. 4 RTL schemtic of UART reception

Fig.5 and Fig.6 are the simulation results of UART transmission and reception. The data_in and data_out is shown with different colour so that the input and output is understood easily. Also the total time required for transmission is shown and it is 86.2µs and time to receive each bit is 8.62µs.

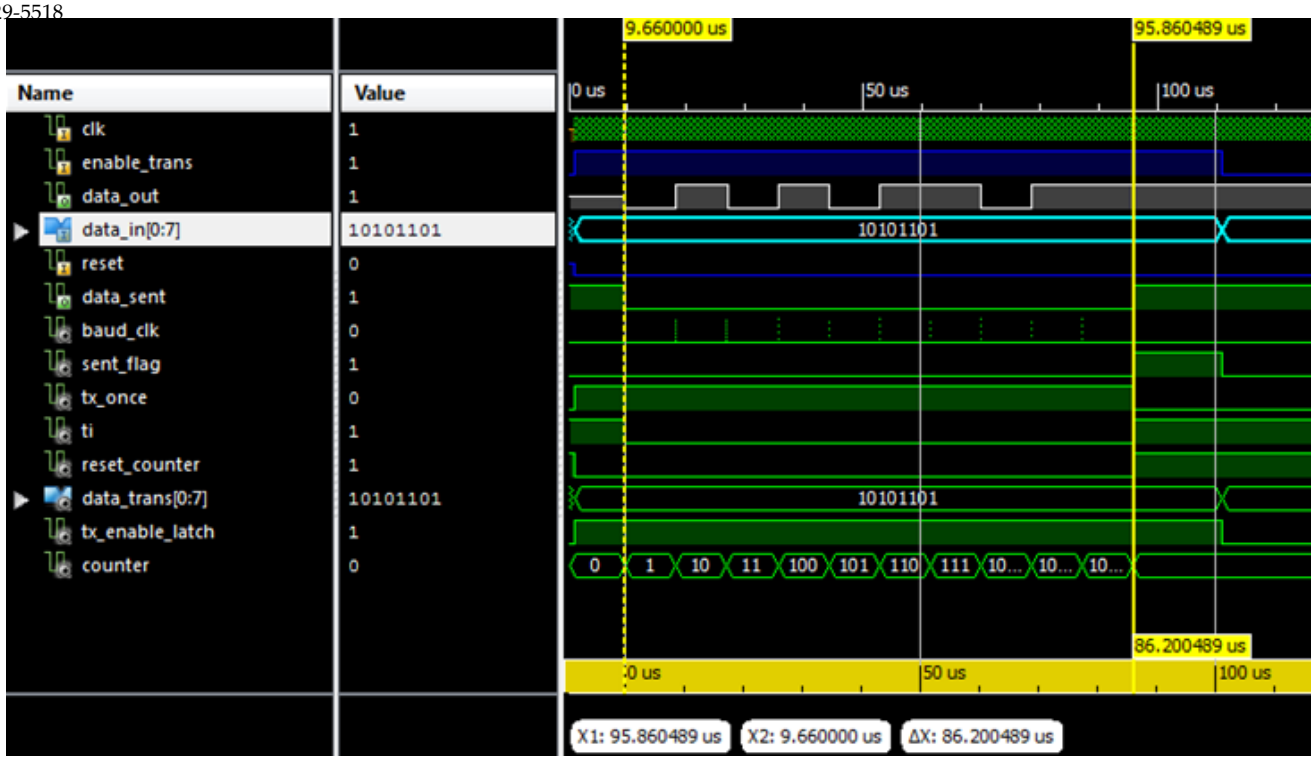

Fig. 5 Simulation Results for UART transmission

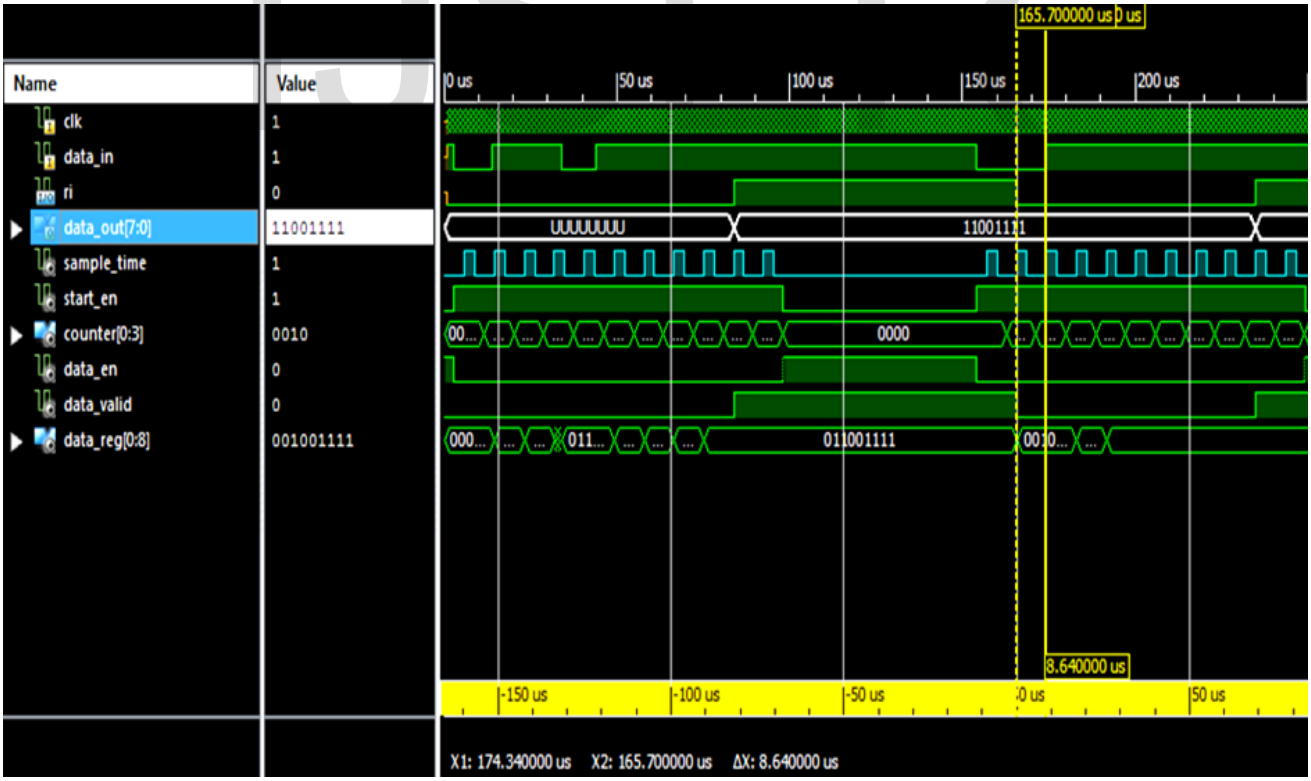

Fig. 6 Simulation Results for UART reception

5 CONCLUSION

UART is design and simulated for the communication between FPGA and TDC. This design uses VHDL as the design language to achieve the modules of UART. Using XILINX 13.9 software for simulation and then it is tested on SPARTAN 6 LX9TQG 144. The results obtained are stable and reliable. The design has high integration, great flexibility, with some refernce value.

ACKNOWLEDGMENT

Authors highly acknowledge the invaluable support by Medical Electronics Department, Society for Applied Microwave Electronics Engineering and Research (Dept. of Information Technology Govt. of India) Mumbai, India.

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